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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,716	09/30/2003	Robert H. Utley	3	6315

7590 02/28/2006

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EXAMINER	
BORKOWSKI, ROBERT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,716	UTLEY, ROBERT H.	
	Examiner	Art Unit	
	Robert Borkowski	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (U.S. Patent No. 5,764,641).

Regarding claims 1, 19-20, Lin discloses, a processor comprising (Fig. 1 element 10):

a plurality of input ports (column 4 lines 51-58, Fig. 1 element 12);

memory circuitry (column 4 lines 51-58, Fig. 1 element 14) for storing data blocks associated with protocol data units and received by the processor at the input ports; and

controller circuitry (column 4 lines 51-58, Fig. 1 element 18) coupled to the memory circuitry and operative to discard (column 5 lines 48-53) certain ones of the data blocks received at the input ports in an oversubscription condition (column 6 lines 37-44 "comparison done by the controller") in which the received data block exceed a designated capacity (column 6 lines 37-44, Fig. 3B step 110) of the processor;

wherein a discarded data block indicator is generated (column 6 lines 45-54, Fig. 3B step 111) for a given one of the input ports if a data block received at the given input

port for a particular protocol data unit is discarded (column 6 line 67 thru column 7 line 8); and

wherein one or more additional data blocks received at the given input port for the particular protocol data unit are discarded (column 6 line 67 thru column 7 line 8 "discard cell") based at least in part on the discarded data block indicator (column 6 line 67 thru column 7 line 8, Fig. 3A-B steps 101 and 112).

Regarding claim 2, Lin discloses wherein the controller circuitry sets the discard data block indicator for the given input port to a first value when a first data block of the particular protocol data unit is discarded (column 6 lines 45-54 "EPD flag").

Regarding claim 3, Lin discloses wherein the controller circuitry is configured to automatically discard any remaining data block if the particular protocol data unit that are received at the given input port while the discarded data block indicator is set to the first value (column 6 line 62 thru column 7 line 8).

Regarding claim 4, Lin discloses wherein the discarded data block indicator for the given input port comprises a single bit (column 6 lines 3-18, Fig. 2 element 36).

Regarding claim 5, Lin discloses wherein the single bit being at a first logic level indicates that at least one data block received at the given input port has been discarded (Fig. 3A-B steps 112-115) for a corresponding protocol data unit (column 6 lines 3-18, lines 45-54, Fig. 3B step 114), and the single bit being at a second logic level indicates that no data block received at the given input port has yet been discarded for the corresponding protocol data unit (column 6 lines 3-18 "CLP bit").

Regarding claim 6, Lin discloses wherein the controller circuitry is operative to maintain a separate discarded data block indicator for each of the plurality of input ports (column 6 lines 55-61, Fig. 3B step 111-112).

Regarding claim 7, Lin discloses wherein the a given one of the discarded data block indicators (column 6 lines 3-18 "CLP bit") indicates whether or not at least one data block received at the corresponding input port has been discarded (column 6 lines 55-61, Fig. 3B step 111-112).

Regarding claim 8 Lin discloses wherein after a final data block of the particular protocol data unit is received (Fig. 3A step 101) at the given input port while the discarded data block indicator for the given input port is set to the first value (column 6 line 62 thru column 7 line 8, Fig. 3A step 101), the controller circuitry is operative to enqueue the particular protocol data unit in a protocol data unit buffer of the memory circuitry (column 7 lines 9-19, Fig. 3A steps 101-106).

Regarding claim 9-10, Lin discloses wherein the particular protocol data unit is enqueued with an associated error flag set (column 7 lines 9-19, Fig. 3A step 103 "CLP=0").

Regarding claim 11, Lin discloses wherein the oversubscription condition is overcome by discarding only data blocks received at the given input port (column 6 lines 37-54 ""stored cells associated with the particular virtual connection"), and associated with the particular protocol data unit (column 6 line 62 thru column 7 line 8, Fig. 3A-B steps 108 and 115).

Regarding claim 12, Lin discloses wherein the received protocol data units (column 5 line 54 thru column 6 line 2, Fig. 2 element 20) are associated with frame-based data (column 5 line 54 thru column 6 line 2, Fig. 2 element 22).

Regarding claim 13-14, Lin discloses wherein at least one of the input ports comprises

a physical input port of the processor (column 4 lines 51-58, Fig. 1 element 12);

a logical input port of the processor (column 3 line 64 thru column 4 line 8, Fig. 1 element 12).

Regarding claim 15, Lin discloses wherein the protocol data unit (Fig. 2 element 20) comprises a packet (column 5 line 54 thru column 6 line 2, Fig. 2 element 22).

Regarding claim 16, Lin discloses wherein the processor is configured to provide an interface for communication of the received protocol data units between a network and a switch fabric (Fig. 1 element 16 the examiner construes the output ports as a switch fabric, because it performs the switching function of routing pockets).

Regarding claim 17, Lin discloses wherein the processor comprises a network processor (column 6 lines 24-36, Fig. 1 element 18, column 4 lines 50-58 " a network").

Regarding claim 18, Lin discloses wherein the processor is configured as an integrated circuit (Fig. 1 element 10).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made of record of to further show the frame discard method for a packet switch.

1) Suzuki et al. U.S. Patent App. Pub. No. 2001/0048662 A1

2) Schwartz et al. U.S. Patent No. 6,434,115 B1

3) Knight et al. U.S. Patent App. Pub. No. 2002/0176424 A1

4) Edsall et al. U.S. Patent App. Pub. No. 2003/0172149 A1

5) Pillar et al. U.S. Patent App. Pub. No. 2003/0202481 A1

6) Maria et al. U.S. Patent No. 6,874,026 B2

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Borkowski whose telephone number is 571-272-8626. The examiner can normally be reached on Monday - Friday 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM NGOC (KIM) HUYNH can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert Borkowski
Art Unit 2181
February 16, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER

2/17/06